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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/789,774	02/27/2004	Joe M. Poss	16869Q-092300US	1897
20350	7590	12/02/2004	EXAMINER	
TOWNSEND AND TOWNSEND AND CREW, LLP TWO EMBARCADERO CENTER EIGHTH FLOOR SAN FRANCISCO, CA 94111-3834			LAXTON, GARY L	
			ART UNIT	PAPER NUMBER
			2838	

DATE MAILED: 12/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/789,774	POSS, JOE M.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Gary L. Laxton	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-30 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-30 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 27 February 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |  |
|--|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. ____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)            |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>2/27/04</u> . | 6) <input type="checkbox"/> Other: ____  |

## **DETAILED ACTION**

### ***Specification***

1. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

### ***Claim Objections***

2. Claims 10, 11, 21, 23 and 28-30 are objected to because of the following informalities:

Claim 10 line 1 recites "an can" [sic].

Claim 10 recites the limitation "a load" in line 4. There is insufficient antecedent basis for this limitation in the claim. A load appears to have been claimed in claim 1 therefore, it is unclear if this is a second load or the same as claimed in claim 1.

Claim 21 line 2 recites "an can" [sic].

Claim 23 recites the limitation "said circuit" in line 10. There is insufficient antecedent basis for this limitation in the claim. Line 2 recited a circuit and line 6 recited a circuit. Which one is the applicant trying to reference?

Claim 28 recites the limitation "said output voltage level" in line 1. There is insufficient antecedent basis for this limitation in the claim.

Claim 23 recites the limitation "said output node" in line 10. There is insufficient antecedent basis for this limitation in the claim. Claims 29 and 30 inherit the same.

***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

4. Claims 1, 6-13 and 20-22 are rejected under 35 U.S.C. 102(a) as being anticipated by Pulkin et al (US 6,573,694).

Claims 1, 6-13 and 20-22; Pulkin et al disclose a regulator circuit comprising; a circuit control node (22); a circuit output node (Vout) to which a load is connected (load), a voltage at the circuit output node being determined based on a voltage signal at the circuit control node; an amplifier circuit (24) having a first amplifier input and a second amplifier input, and further having an amplifier output, the first amplifier input configured for receiving a reference voltage (VREF), the amplifier circuit (24) receiving power from a first voltage source (Vs); a source follower circuit (34) having a source follower input node and a source follower output, the amplifier output configured drive the source follower input node, the source follower output coupled to the circuit control node; and a feedback circuit (26, 28) coupled between the circuit output node and the second amplifier input. Pass element (22). Current source (32)

5. Claims 2, 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pulkin et al (US 6,573,694) in view of Hsiao et al (US 3,984,780).

Pulkin et al disclose the claimed subject matter in regards to claims 1 and 12 supra, except for a current mirror coupled between the amplifier and the source follower.

Hsiao et al teaches a source follower (4) and an amplifier (2) having a current mirror coupled (32) therebetween for mirroring the current from the amplifier to regulate the output voltage.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Pulkin et al to include a current mirror coupled between the amplifier and the source follower for mirroring the amplifier current and regulating the output voltage as taught by Hsiao et al.

6. Claims 3-5, 14 and 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pulkin et al (US 6,573,694) and Hsiao et al (US 3,984,780) in view of Miranda et al (US 5,631,598).

Pulkin et al and Hsiao et al disclose the claimed subject matter in regards to claims 1 and 12 supra, except for a resistor component coupled between a voltage source and the source follower input.

Miranda et al teach connecting a resistor component (R3, R4) between a voltage rail and a transistor for among other things restricting current to the transistor and dividing the source voltage.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Pulkin et al and Hsiao et al to include a resistor component coupled between a voltage source and the source follower input in order to restrict current therethrough or to divide the source voltage to a proper voltage for the source follower input.

***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 23, 28 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pulkin et al (US 6,573,694) in view of Xi (US 6,246,221).

Pulkin et al disclose a regulator circuit comprising; an amplifier circuit (24), a first amplifier input configured for receiving a reference voltage (VREF), the amplifier circuit (24) receiving power from a first voltage source ( $V_S$ ); a source follower circuit (34) having a source follower input node and a source follower output, the amplifier output configured drive the source follower input node, the source follower output coupled to the circuit control node; and a feedback circuit (26, 28) coupled between the circuit output node and the second amplifier input. Pass element (22).

However, Pulkin et al do not disclose a bandwidth at the output node has a pole at a frequency greater than the unity gain frequency of the circuit.

Xi teaches an output amplifier stage having a pole associated therewith, the output amplifier stage configured to receive the amplified displacement current signal such that the pole associated with the output amplifier stage is pushed out to a frequency above the Unity Gain Frequency of the compensation loop thereby rendering the voltage regulator output stage capable of generating a stable regulated output voltage at frequencies in the vicinity of the control loop bandwidth associated with the voltage regulator.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Pulkin et al to include a bandwidth at the output node has a pole at a frequency greater than the unity gain frequency of the circuit as taught by Xi in order to render the voltage regulator output stage capable of generating a stable regulated output voltage at frequencies in the vicinity of the control loop bandwidth associated with the voltage regulator.

9. Claims 24-27 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pulkin et al (US 6,573,694) and Xi (US 6,246,221) in view of Miranda et al (US 5,631,598).

Pulkin et al and Xi disclose the claimed subject matter in regards to claim 23 supra, except for a resistor component coupled between a voltage source and the source follower input.

Miranda et al teach connecting a resistor component (R3, R4) between a voltage rail and a transistor for among other things restricting current to the transistor and dividing the source voltage.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Pulkin et al and Hsiao et al to include a resistor component coupled between a voltage source and the source follower input in order to restrict current therethrough or to divide the source voltage to a proper voltage for the source follower input.

### ***Conclusion***

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US 6,586,987 Somerville et al disclose an op amp, current mirror

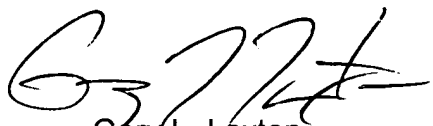
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and source follower circuit; US 6,646,495 Perez discloses an op amp, source follower and pass device.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gary L. Laxton whose telephone number is (571) 272-2079. The examiner can normally be reached on Monday thru Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on (571) 272-2084. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

 11/29/04  
Gary L. Laxton  
Patent Examiner  
Art Unit 2838